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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,754	08/20/2001	Mohan Kalkunte	108339-00026	6943
32294	7590	04/21/2005	EXAMINER	
SQUIRE, SANDERS & DEMPSEY L.L.P.			GREY, CHRISTOPHER P	
14TH FLOOR			ART UNIT	
8000 TOWERS CRESCENT			PAPER NUMBER	
TYSONS CORNER, VA 22182			2667	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/931,754

Applicant(s)

KALKUNTE ET AL.

Examiner

Christopher P Grey

Art Unit

2667

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Drawings

1. The drawings are objected to because:
 - (a) Page 7 and 10 disclose an external memory 12 not shown within any of the drawings
 - (b) Page 7 discloses elements 81, 82 and 83 not labeled within any of the drawings
 - (c) Page 8 discloses Ethernet ports 13 not labeled within any of the drawings
 - (d) Page 9 discloses a submodule 14 not labeled within any of the drawings

Appropriate correction is required

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant et al. (US 6625146) in view of Denio et al. (US 6556575)

Claim 1 Merchant et al. ('Merchant' hereinafter) discloses a network multiport switch for network communications (see fig 3A) comprising a number of data ports for transmitting and receiving data at a number of possible wire rates (Col 7 lines 15-25 and Col 3 lines 53-60).

Merchant discloses a CPU interface (element 50 in Fig 2) configured to communicate with a CPU (Col 6 lines 1-25 and Col 4 lines 48-61).

Merchant discloses receive and transmit buffers (Col 5 lines 32-42) that act as the internal memory.

Merchant discloses an external memory for storing data via an external memory interface controller. Merchant also discloses a scheduler for controlling memory access (Col 7 lines 1-25).

Merchant discloses a communication channel (element 69 in fig 2) for communicating data to and from a number of components.

Merchant discloses an IRC (element 40) that monitors data by determining header information that includes source and destination addresses (Col 5 lines 43-67).

Merchant discloses forwarding and discarding data as necessary (see fig 10A). However Merchant does not disclose a fast filtering processor filtering the data coming into one data port interface and taking selective filtering action based upon a filtering result.

Denio et al. ('Denio' hereinafter) discloses a switching device comprising a forwarding module (Fast filtering processor) for filtering packet incoming from a number of ports (Col 4 lines 55-Col 5 lines2). Based on the filtering action, the forwarding module forwards packets in accordance to a switching algorithm or forwards packets to a data processor (selective filter action) as disclosed in Col 3 lines 12-29.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the operation of forwarding/discarding of data in a switching device

with a forwarding module (filter) containing rules in order to reduce traffic (Col 5 lines 47-50).

Claim 2 Merchant discloses a CPU and CPU interface as disclosed in the rejection of claim 1. The CPU controls a management entity (Col 4 lines 47-60). However Merchant does not specifically disclose fast filtering processor being programmable by the CPU.

Denio discloses the forwarding module (filter) accessing a look-up table (Col 5 lines 3-19), where it would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the CPU which is connected to a rules table as disclosed by Merchant with the operations of the forwarding module as disclosed by Denio. The motivation for this combination is to allow a user to adjust filtering scenarios (Col 5 lines 3-19).

Claim 3 Merchant discloses a rules checker accessing an address table (Col 9 lines 16-22) and an indexed rules table (Col 10 lines 1-16). Merchant does not disclose a fast filtering processor applying a filtering mask to a packet, providing a filter result, applying the filter result to predetermined rules in the indexed rules table, and flows of data are updated based upon the filtering.

Denio discloses a fast filtering processor as disclosed in the rejection of claim 1. Furthermore Denio discloses creating a filtering mask (Col 6 lines 30-36).

Denio discloses determining whether or not filtering/forwarding heuristics (rules) apply, and from that result forwarding packets to apply forwarding heuristics (Col 6 lines 54-67), and a new forwarding mask is created (updated).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to implement the indexed table as disclosed by Merchant with the result of filtering as disclosed by Denio in order to allow for greater traffic reduction (Col 5 lines 46-50).

Claim 4 Merchant discloses a switching device, where switching devices are commonly implemented on semiconductor substrates (inherent). Furthermore the rejection of claim 1 discloses the components within the switching device.

Claim 5 Merchant does not disclose the fast filtering processor including a set of exclusive filter masks and inclusive filter masks, where the exclusive filter masks are configured to exclude all packets with which there is a match with the filter results.

Denio discloses creating filter masks as disclosed in the rejection of claim 3. Denio discloses filtering heuristics being either inclusive or exclusive, where the exclusive rules specify not to forward packets that are not known (do not match) as disclosed in Col 5 lines 36-65.

Claim 6 Merchant does not disclose filter masks which filter ingress and egress port fields and filter select fields of an incoming packet.

Denio discloses filter masks where the first two bits represent input and output ports and all other filtered bits are acknowledged by 1's (Col 6 lines 30-43).

Claim 7 Merchant discloses the IRC containing an indexed table as disclosed in the rejection of claim 3. The internal rules checker (IRC) accesses a number of tables and outputs a forwarding descriptor containing priority class information, port information (ingress and egress) and other information (Col 6 lines 1-25) necessary to

forward data. It would have been obvious to one of the ordinary skill in the art at the time of the invention that a number of different fields can be included within the table depending on the users specifications.

Claim 8 Merchant discloses an indexed table containing port to index information (Col 10 lines 1-17) and a lookup logic (Col 9 lines 15-22), where the IRC accesses the table in order to monitor destination and source addresses (Col 5 lines 43-67).

Claim 9 The fast filtering processor filters the packets as disclosed in the rejection of claim 1. Furthermore Merchant discloses operation in a CPU-less environment (Col 12 lines 64-Col 13 line 20).

Claim 10, 13 Merchant discloses queuing logic (elements 74 in fig 3) for queuing incoming packets (Col 7 lines 1-14).

Merchant discloses an internal rules checker (Col 5 lines 43-67), where located within is an address table and address lookup logic (Col 9 lines 15-22).

Merchant discloses an address lookup logic accessing an address table and determining VLAN index identifiers (Col 9 lines 15-41).

Merchant also discloses a port to index table within the IRC (Col 10 lines 1-16).

Merchant discloses a decision making engine for determining the forwarding or discarding of packets. However Merchant does not disclose the fast filtering processor for filtering incoming packets in order to determine what specific actions should be taken to further modify the packet handling.

Denio discloses a switching device comprising a forwarding module (Fast filtering processor) for filtering packets incoming from a number of ports (Col 4 lines 55-Col 5 lines2).

Denio discloses a number of rules that defines the filtering, where packets may be forwarded or discarded appropriately (Col 5 lines 35-65).

Therefore it would have been obvious to one of the ordinary skill in the art at the time of the invention to implement the forwarding module disclosed by Denio giving access to the IRC and the tables contained within, as disclosed by Merchant. The motivation for this implementation is to reduce the traffic congestion (Col 5 lines 47-50).

Claim 11, 14 Merchant discloses an IRC that monitors header information of an incoming packet, including source and destination addresses (Col 5 lines 43-67).

Claim 12, 15 Merchant discloses source and destination addresses that are related to the received packets as disclosed in the rejection of claim 11. Merchant also discloses the IRC monitoring incoming packets (Col 5 lines 43-67).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Kadambi et al. (US 6335935) discloses within claim 1 all of the limitations of the present application except for a flow monitor, which is questionable for further limiting the claimed invention.

(b) Hill et al. (US 5796944) discloses an address management circuit and method of operation that includes a search engine for searching an address table for source and destination address.

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4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 6:30-3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571)272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher Grey
Examiner
Art Unit 2667

C. Grey
4/6/05

A. Qureshi 4/6/05

**AFSAR QURESHI
PRIMARY EXAMINER**